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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
VANNUCCI, JAMES	

ART UNIT	PAPER NUMBER
2828	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,923	HWANG, HONG-GIE	
	Examiner	Art Unit	
	Jim Vannucci	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,18-22,33 and 34* is/are rejected.

7)☒ Claim(s) *11-17 and 23-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 7 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al.(6,775,216) in view of Alon et al.(5,701,283).

Claim 1, figure 9A of Kely discloses generating an error voltage(VMDC) between an output voltage(PDO) of a laser diode(70) sampled during an automatic power control period and a reference voltage(280).

Kelly discloses processing the error voltage(302) into a compensated control voltage and applying it to a laser diode(70), but does not disclose using proportional-integral processing on the error voltage.

Alon discloses performing proportional-integral processing(col. 8, equ. 1) on a voltage signal to generate a compensated control voltage that is more smoothed and averaged out(col. 8, lines 20-50).

Claim 2, the output voltage(PDO) disclosed in figure 9A of Kelly is an effective output voltage within a predetermined range(set by the amplifier 306).

Claim 3, the compensated control voltage applied to the laser diode(70) is an effective control voltage within a predetermined range(set by the amplifier 288).

Claim 7, figure 9A of Kelly discloses generating an error voltage(VWDC) between an output voltage of a laser diode sampled during an automatic power control period and a reference voltage, and processing the error voltage to generate a compensated control voltage and applying the compensated control voltage to the laser diode(70). Column 8 of Alon discloses performing proportional-integral processing on a signal voltage.

Claim 9, figure 9A of Kelly discloses an error voltage generation unit generating an error voltage(VWDC) between an output voltage(362) of a laser diode sampled during an automatic power control period and a reference voltage(286), and a control voltage generation unit(302) processing the error voltage to generate an effective control voltage. Column 8 of Alon discloses a unit performing proportional-integral processing on a voltage signal.

Claim 10, figure 8 of Oku discloses an analog-to-digital converter(30) converting the output voltage of a laser diode from an analog form to a digital form, and an effective output voltage extractor(18) extracting an effective output voltage from the digital output voltage provided from the analog-to-digital converter. Figure 9A of Kelly discloses a subtractor(288) subtracting a reference voltage from the effective output voltage provided from the effective output voltage extractor to generate the error voltage.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the processing steps disclosed in Alon with the processing steps disclosed in Kelly to smooth out the signal as disclosed in Alon.

3. Claims 4-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oku(5,222,072) in view of Kelly, and further in view of Alon.

Claim 4, Figure 8 of Oku discloses setting an automatic power control period(set by 14) for a laser diode, converting(30) an output voltage(29) of the laser diode from an analog form to a digital form, and converting(25 & 26) an effective control voltage from the digital form to the analog form.

Oku does not disclose generating an error voltage or proportional integral processing.

Figure 9A of Kelly discloses generating an error voltage(VWDC) between a reference voltage and an effective output voltage extracted from output voltages sampled during the automatic power control period(fig. 10) and generating an effective control voltage using a compensated control voltage to determine the write power needed in a disk drive system(abstract).

Column 8 of Alon discloses performing proportional-integral processing on an error voltage to generate a control voltage for improved signal smoothing.

Claim 5, figure 8 of Oku discloses sampling(22) the digital output voltage of a laser diode(29) during an automatic power control period and extracting the sampled digital output voltage that exists within a range between a first maximum and a first minimum as the effective output voltage(A1). Column 8 of Alon discloses calculating an average effective output voltage. Figure 9A of Kelly discloses generating the error voltage between the average effective output voltage and the reference voltage.

Claim 6, Column 8 of Alon discloses performing a proportional integral process to average out the value of a signal. Figure 9A of Kelly discloses processing an the error voltage(VWDC) to generate a compensated control voltage that exists within a range between a second maximum and a second minimum as the effective control voltage.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use an error voltage as disclosed in Kelly and proportional integral processing as disclosed in Alon with the device disclosed in Oku for improved start up operation as disclosed in Kelly(col. 2) and for a more smoothed out signal as disclosed in Alon.

4. Claims 18, 20-21 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al.(5,276,781) in view of Kelly, and further in view of Alon.

Claims 18 and 33-34, figures 1 and 2 of Chang discloses a laser printer controller(12) structured in a single integrated circuit, an engine processor module(20) and a power control module(fig. 2).

Chang does not disclose the specific recited limitations concerning the power control module.

Figure 9A of Kelly discloses an automatic power control module for a laser diode(70) automatically controlling an output power of the laser diode positioned within a laser scanning unit by sampling an effective output voltage from an output power of the laser diode during a automatic power control period.

Chang and Kelly do not disclose the recited processing method.

Column 8 of Alon discloses performing proportional-integral processing on a voltage to smooth out the signal.

Claim 20, figure 1 of Chang discloses an engine processor module(20) controlling an operation of a printer engine, and a power control module(12).

Figure 9A of Kelly discloses an automatic power control module automatically controlling an output power of the laser diode by generating an error voltage between an output voltage of the laser diode sampled during an automatic power control period and a reference voltage, and processing the error voltage to generate a compensated control voltage and applying the compensated control voltage to the laser diode.

Column 8 of Alon discloses performing proportional-integral processing on a signal.

Claim 21, figure 9A of Kelly discloses an error voltage generation unit generating the error voltage between the output voltage of the laser diode, which is extracted for a duration of the automatic power control period, and the reference voltage.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use an error voltage as disclosed in Kelly and proportional integral processing as disclosed in Alon with the device disclosed in Chang for improved start up operation as disclosed in Kelly(col. 2) and for a more smoothed out signal as disclosed in Alon.

5. Claims 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Kelly and Alon as referenced above, and further in view of Oku.

Chang, Kelly and Alon do not disclose A/D and D/A converters as recited in these claims.

Claim 19, figure 8 of Oku discloses an analog-to-digital converter(30) converting the output voltage of the laser diode from an analog form to a digital form, and a digital-to-analog converter(25 or 26) converting a control voltage from the digital form to the analog form.

Figure 9A of Kelly discloses an error voltage generation unit generating an error voltage between a reference voltage and the effective output voltage selected from digital output voltages extracted during the automatic power control period, and generating a compensated control voltage and an effective control voltage using the compensated control voltage.

Column 8 of Alon discloses a control unit performing proportional-integral processing on a voltage.

Claim 22, figure 8 of Oku discloses an analog-to-digital converter(30) converting a voltage of an output power of a laser diode to a digital output voltage.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the converters disclosed in Oku with the device disclosed in Chang, Kelly and Alon for converting signals between digital and analog format as disclosed in Oku.

Allowable Subject Matter

6. Claims 11-17 and 23-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter. The following limitations are primarily responsible for distinguishing these claims over the prior art.

Regarding claims 11, 13 and 15-17, the limitations concerning a sampler sampling the digital output voltage provided from the analog-to-digital converter during the automatic power control period, a comparator comparing the sampled output voltage with a first maximum and a first minimum, determining whether the sampled output voltage exists within an effective range defined by the first maximum and the first minimum, and extracting the effective output voltage within the effective range, an accumulator accumulating the effective output voltage extracted by the comparator, and a divider dividing the accumulated effective output voltage by a number of accumulations to obtain an average effective output voltage as recited in claim 11.

Regarding claims 12 and 14, the limitations concerning a sampler controlling the analog-to-digital converter to perform conversion only during the automatic power control period, a comparator comparing the output voltage provided from the sampler with a first maximum and a first minimum, determining whether the sampled output voltage exists within an effective range defined by the first maximum and the first minimum, and extracting the effective output voltage within the effective range; an

accumulator accumulating the effective output voltage extracted by the comparator, and a divider dividing the accumulated effective output voltage by a number of accumulations to obtain an average effective output voltage as recited in claim 12.

Regarding claims 23-32, the limitations concerning a sampler sampling the digital output voltage from the analog-to-digital converter during the automatic power control period, a first comparator setting a first maximum and a first minimum to define an effective range of the digital output voltage of the laser diode, comparing the first maximum and the first minimum with the sampled digital output voltage received from the sampler, determining whether the sampled digital output voltage exists within the effective range, and outputting an effective output voltage, an accumulator accumulating the effective output voltage, and a first divider dividing an accumulated result output from the accumulator by a number of accumulations to calculate an average effective output voltage as recited in claim 23.

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Jim Vannucci whose phone number is (571) 272-1820.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center whose telephone number is (703) 308-0956.

Papers related to Technology Center 2800 applications only may be submitted to Technology Center 2800 by facsimile transmission. Any transmission not to be

considered an official response must be clearly marked "DRAFT". The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center Fax Center number is (703) 872-9306.

James Vannucci

James Vannucci